What is claimed is:

1. A field-effect transistor comprising:

first and second conductive layers separated by an interlayer dielectric layer; and

a conductive strap disposed on each of opposing sidewalls of the field-effect transistor, wherein each strap electrically interconnects the first and second conductive layers.

2. The field-effect transistor of claim 1, wherein the first and second conductive layers are of polysilicon.

3. The field-effect transistor of claim 1, wherein each strap comprises metal.

4. The field-effect transistor of claim 1, further comprising a dielectric layer underlying the first conductive layer and overlying a substrate.

5. The field-effect transistor of claim 4, further comprising a third conductive layer overlying the second conductive layer, each strap contacting the third conductive layer.

6. The field-effect transistor of claim 5, further comprising a cap layer disposed on the third conductive layer, wherein each strap extends substantially from an upper surface of the cap layer to the first conductive layer.

7. A field-effect transistor comprising:

a first dielectric layer disposed on a substrate;

a first polysilicon layer disposed on the tunnel dielectric layer;

a second dielectric layer disposed on the first polysilicon layer;

a second polysilicon layer disposed on the second dielectric layer;

a metal-containing layer disposed on the second polysilicon layer; and

a metal-containing strap disposed on each of opposing sidewalls of the field-effect transistor, wherein each strap electrically interconnects the first and second polysilicon layers.

8. The field-effect transistor of claim 7, wherein metal-containing layer comprises a material selected from the group consisting of refractory metals and refractory metal silicides.

9. The field-effect transistor of claim 7, further comprising a cap layer disposed on the metal layer, wherein each metal strap extends substantially from an upper surface of the cap layer to the first polysilicon layer.

10. The field-effect transistor of claim 9, wherein the cap layer is a layer of tetraethylorthosilicate.

11. A NAND memory array comprising:

a plurality of rows of memory cells, each row connected to a word line; and

a plurality of columns of NAND strings of memory cells, each NAND string selectively connected to a bit line through a first select gate of the respective

column, the first select gate of the respective columns interconnected by a first select line, each of the first select gates and the first select line comprising:

first and second conductive layers separated by an interlayer dielectric layer; and

a pair of opposing conductive straps, wherein each strap electrically interconnects the first and second conductive layers, and wherein the pair of opposing straps spans two or more of the plurality of columns.

12. The NAND memory array of claim 11, wherein the first and second conductive layers are of polysilicon.

13. The NAND memory array of claim 11, wherein each strap comprises metal.

14. The NAND memory array of claim 11, further comprising a dielectric layer underlying the first conductive layer and overlying a substrate.

15. The NAND memory array of claim 14, further comprising a third conductive layer overlying the second conductive layer, each strap contacting the third conductive layer.

16. The NAND memory array of claim 15, further comprising a cap layer disposed on the third conductive layer, wherein each strap extends substantially from an upper surface of the cap layer to the first conductive layer.

17. The NAND memory array of claim 11, wherein each NAND string is selectively connected to a source line through a second select gate of the respective column, the second select gate of the respective columns interconnected by a second select line, each of the second select gates and the second select line comprising:

first and second conductive layers separated by an interlayer dielectric layer; and

a pair of opposing conductive straps, wherein each strap electrically interconnects the first and second conductive layers, and wherein the pair of opposing straps spans two or more of the plurality of columns.

18. The NAND memory array of claim 17, wherein the first and second select gates and the first and second select lines are formed concurrently.

19. A NAND memory array comprising:

a plurality of rows of memory cells, each row connected to a word line; and

a plurality of columns of NAND strings of memory cells connected between source select gates and drain select gates, each column coupled to a bit line, each of the source and drain select gates and each of the memory cells comprising:

a first dielectric layer disposed on a substrate;

a first polysilicon layer disposed on the first dielectric layer;

a second dielectric layer disposed on the first polysilicon layer;

a second polysilicon layer disposed on the second dielectric layer; and

a metal-containing layer disposed on the second polysilicon layer;

wherein each of the source and drain select gates further comprises a pair of opposing first conductive straps respectively disposed on each of

opposing sidewalls of each of the source and drain select gates, wherein each first conductive strap electrically interconnects the first and second polysilicon layers, the pair of opposing first conductive straps spanning two or more of the plurality of columns; and

wherein each of the memory cells further comprises a pair of opposing second conductive straps respectively disposed on each of opposing sidewalls of each of the memory cells, wherein each second conductive strap contacts the metal-containing layer and the second polysilicon layer and extends to the second dielectric layer, the pair of opposing second conductive straps spanning two or more of the plurality of columns.

20. The NAND memory array of claim 19, wherein each of the source and drain select gates and each of the memory cells further comprises a cap layer disposed on the metal-containing layer, wherein each first conductive strap extends substantially from an upper surface of the cap layer of each of the source and drain select gates to the first polysilicon layer and wherein each second conductive strap extends substantially from an upper surface of the cap layer of each of the memory cells to the second dielectric layer.

21. The field-effect transistor of claim 20, wherein the cap layer is a layer of tetraethylorthosilicate.

22. A floating-gate transistor comprising:

a tunnel dielectric layer disposed on a substrate;

a floating gate layer disposed on the tunnel dielectric layer;

an interlayer dielectric layer disposed on the floating gate layer;

a control gate layer disposed on the interlayer dielectric layer; and

a conductive strap disposed on each of opposing sidewalls of the floating-gate transistor, wherein each strap contacts the control gate layer and extends substantially from an upper surface of the floating-gate transistor to the interlayer dielectric layer.

23. The floating-gate transistor of claim 22, further comprising a cap layer disposed on the control gate layer, wherein each strap extends substantially from an upper surface of the cap layer to the interlayer dielectric layer.

24. A floating-gate transistor comprising:

a tunnel dielectric layer disposed on a substrate;

a first polysilicon layer disposed on the tunnel dielectric layer;

an interlayer dielectric layer disposed on the first polysilicon layer;

a second polysilicon layer disposed on the interlayer dielectric layer;

a metal-containing layer disposed on the second polysilicon layer; and

a metal-containing strap disposed on each of opposing sidewalls of the floating-gate transistor, wherein each strap contacts the metal-containing layer and the second polysilicon layer and extends substantially from an upper surface of the floating-gate transistor to the interlayer dielectric layer.

25. The floating-gate transistor of claim 24, further comprising a cap layer disposed on the metal-containing layer, wherein each strap extends substantially from an upper surface of the cap layer to the interlayer dielectric layer.

26. The floating-gate transistor of claim 25, wherein the cap layer is a layer of tetraethylorthosilicate.

27. A memory array comprising:

a plurality of floating-gate memory cells arranged in rows and columns, each floating-gate memory cell comprising:

a tunnel dielectric layer disposed on a substrate;

a floating gate layer disposed on the tunnel dielectric layer;

an interlayer dielectric layer disposed on the floating gate layer;

a control gate layer disposed on the interlayer dielectric layer; and

a conductive strap disposed on each of opposing sidewalls of the floating-gate transistor, wherein each strap contacts the control gate layer and extends substantially from an upper surface of the floating-gate transistor to the interlayer dielectric layer, wherein each strap further spans two or more columns of memory cells.

28. The memory array of claim 27, further comprising a cap layer disposed on the control gate layer, wherein each strap extends substantially from an upper surface of the cap layer to the interlayer dielectric layer.

29. A memory device comprising:

a memory array comprising:

a plurality of rows of memory cells, each row connected to a word line; and

a plurality of columns of NAND strings of memory cells connected, each NAND string selectively connected to a bit line through a select gate of the respective column, the select gates of the respective columns

interconnected by a select line, each of the select gates and the select line comprising:

first and second conductive layers separated by an interlayer dielectric layer; and

a pair of opposing conductive straps, wherein each strap electrically interconnects the first and second conductive layers, and wherein the pair of opposing straps spans two or more of the plurality of columns;

column access circuitry connected to the bit lines; and

row access circuitry connected to the word lines.

30. A memory device comprising:

a memory array comprising:

a plurality of rows of memory cells, each row connected to a word line; and

a plurality of columns of NAND strings of memory cells connected between source select gates and a drain select gates, each column selectively coupled to a bit line through one of the drain select gates, each of the source and drain select gates and each of the memory cells comprising:

a first dielectric layer disposed on a substrate;

a first polysilicon layer disposed on the first dielectric layer;

a second dielectric layer disposed on the first polysilicon layer;

a second polysilicon layer disposed on the second dielectric layer;

a metal-containing layer disposed on the second polysilicon layer; and

a cap layer disposed on the metal-containing layer;

wherein each of the source and drain select gates further comprises a pair of opposing first conductive straps respectively disposed on each of opposing sidewalls of each of the source and drain select gates, wherein each first conductive strap electrically interconnects the first and second polysilicon layers, contacts the metal-containing layer, and extends substantially from an upper surface of the cap layer of each of the source and drain select gates to the first polysilicon layer, the pair of opposing first conductive straps spanning two or more of the plurality of columns; and

wherein each of the memory cells further comprises a pair of opposing second conductive straps respectively disposed on each of opposing sidewalls of each of the memory cells, wherein each second conductive strap contacts the metal-containing layer and the second polysilicon layer and extends substantially from an upper surface of the cap layer of each of the memory cells to the second dielectric layer, the pair of opposing second conductive straps spanning two or more of the plurality of columns;

column access circuitry connected to the bit lines; and

row access circuitry connected to the word lines.

31. A memory device comprising:

an array of floating-gate memory cells arranged in rows and columns; and

a field-effect transistor located at a periphery of the array and electrically connected to the array, the field-effect transistor and each of the memory cells comprising:

a first dielectric layer disposed on a substrate;

a first conductive layer disposed on the first dielectric layer;

a second dielectric layer disposed on the first conductive layer;

a second conductive layer disposed on the second dielectric layer; and

a third conductive layer disposed on the second conductive layer;

wherein the field-effect transistor further comprises a pair of opposing first conductive straps respectively disposed on each of opposing sidewalls of the field-effect transistor, wherein each first conductive strap electrically interconnects the first and second conductive layers and contacts the third conductive layer; and

wherein each of the memory cells further comprises a pair of opposing second conductive straps respectively disposed on each of opposing sidewalls of each of the memory cells, wherein each second conductive strap contacts the second and third conductive layers and extends to the second dielectric layer, the pair of opposing second conductive straps spanning two or more of the columns.

32. The memory device of claim 31, wherein the first and second conductive layers are polysilicon layers.

33. The memory device of claim 31, wherein the third conductive layer comprises metal.

34. The memory device of claim 31, wherein the field-effect transistor and each of the memory cells further comprises a cap layer disposed on the third conductive layer, wherein each first conductive strap extends substantially from an upper surface of the cap layer of the field-effect transistor to the first conductive layer and wherein

each second conductive strap extends substantially from an upper surface of the cap layer of each of the memory cells to the second dielectric layer.

35. The memory device of claim 31, wherein the array of floating-gate memory cells is a NOR memory array.

36. A memory device comprising:

an array of floating-gate memory cells arranged in rows and columns; and

a field-effect transistor located at a periphery of the array and electrically connected to the array, the field-effect transistor and each of the memory cells comprising:

a first dielectric layer disposed on a substrate;

a first polysilicon layer disposed on the tunnel dielectric layer;

a second dielectric layer disposed on the first polysilicon layer;

a second polysilicon layer disposed on the second dielectric layer; and

a metal-containing layer disposed on the second polysilicon layer;

wherein the field-effect transistor further comprises a pair of opposing first conductive straps respectively disposed on each of opposing sidewalls of the field-effect transistor, wherein each first conductive strap electrically interconnects the first and second polysilicon layers and contacts the metal-containing layer; and

wherein each of the memory cells further comprises a pair of opposing second conductive straps respectively disposed on each of opposing sidewalls of each of the memory cells, wherein each second conductive strap contacts the metal-containing layer and the second polysilicon layer and extends to the second dielectric layer, the pair

of opposing second conductive straps spanning two or more of the columns.

37. The memory device of claim 36, wherein the field-effect transistor and each of the memory cells further comprises a cap layer disposed on the metal-containing layer, wherein each first conductive strap extends substantially from an upper surface of the cap layer of the field-effect transistor to the first polysilicon layer and wherein each second conductive strap extends substantially from an upper surface of the cap layer of each of the memory cells to the second dielectric layer.

38. A memory device comprising:

an array of floating-gate memory cells arranged in rows and columns;

column access circuitry having field-effect transistors connected to the columns; and

row access circuitry having field-effect transistors connected to the rows;

wherein each of the field-effect transistors and each of the memory cells comprises:

a first dielectric layer disposed on a substrate;

a first conductive layer disposed on the first dielectric layer;

a second dielectric layer disposed on the first conductive layer;

a second conductive layer disposed on the second dielectric layer;

a third conductive layer disposed on the second conductive layer; and

a cap layer disposed on the third conductive layer;

wherein each field-effect transistor further comprises a pair of opposing first conductive straps respectively disposed on each of opposing sidewalls of each field-effect transistor, wherein each first conductivestrap electrically interconnects the first and second

conductive layers, contacts the third conductive layer, and extends substantially from an upper surface of the cap layer of each field-effect transistor to the first conductive layer; and

wherein each of the memory cells further comprises a pair of opposing second conductive straps respectively disposed on each of opposing sidewalls of each of the memory cells, wherein each second conductive strap contacts the third conductive layer and the second conductive layer and extends substantially from an upper surface of the cap layer of each of the memory cells to the second dielectric layer, the pair of opposing second conductivestraps spanning two or more of the plurality of columns.

39. A memory device comprising:

an array of floating-gate memory cells arranged in rows and columns;

column access circuitry having field-effect transistors connected to the columns; and

row access circuitry having field-effect transistors connected to the rows;

wherein each of the field-effect transistors and each of the memory cells comprises:

a first dielectric layer disposed on a substrate;

a first polysilicon layer disposed on the first dielectric layer;

a second dielectric layer disposed on the first polysilicon layer;

a second polysilicon layer disposed on the second dielectric layer;

a metal-containing layer disposed on the second polysilicon layer; and

a cap layer disposed on the metal-containing layer;

wherein each field effect transistor further comprises a pair of opposing first conductive straps respectively disposed on each of opposing

sidewalls of each of each field effect transistor, wherein each first conductive strap electrically interconnects the first and second polysilicon layers, contacts the metal-containing layer, and extends substantially from an upper surface of the cap layer of each field effect transistor to the first polysilicon layer; and

wherein each of the memory cells further comprises a pair of opposing second conductive straps respectively disposed on each of opposing sidewalls of each of the memory cells, wherein each second conductive strap contacts the metal-containing layer and the second polysilicon layer and extends substantially from an upper surface of the cap layer of each of the memory cells to the second dielectric layer, the pair of opposing second conductive straps spanning two or more of the plurality of columns.

40. A method of forming a field-effect transistor, comprising:

separating first and second conductive layers of the field-effect transistor with an interlayer dielectric layer; and

electrically connecting the first and second conductive layers using opposing conductive straps formed on either side of the first and second conductive layers and interlayer dielectric layer, thereby forming a control gate of the field-effect transistor.

41. The method of claim 40, wherein the first and second conductive layers are of polysilicon.

42. The method of claim 40, wherein each strap comprises metal.

43. The method of claim 40, further comprising forming the first conductive layer on a gate dielectric layer overlying a substrate.

44. The method of claim 43, further comprising forming a metal-containing layer overlying the second conductive layer before forming the opposing straps.

45. The method of claim 44, further comprising forming a cap layer on the metal-containing layer before forming the opposing straps.

46. A method of forming a field-effect transistor, comprising:

forming a first dielectric layer on a substrate;

forming a first polysilicon layer on the first dielectric layer;

forming a second dielectric layer on the first polysilicon layer;

forming a second polysilicon layer on the second dielectric layer;

forming a metal-containing layer on the second polysilicon layer;

forming a cap layer on the metal-containing layer;

patterning the cap layer, second conductive layer, and second dielectric layer to define a control gate of the field-effect transistor; and

forming a conductive strap on each opposing sidewalls of the control gate so that each strap electrically interconnects the first and second polysilicon layers.

47. A method of forming a field-effect transistor, comprising:

forming a gate dielectric layer overlying a substrate;

forming a first conductive layer overlying the gate dielectric layer;

forming an interlayer dielectric layer overlying the first conductive layer;

forming a second conductive layer overlying the interlayer dielectric layer;

forming a cap layer overlying the second conductive layer;

patterning the cap layer, second conductive layer and interlayer dielectric layer to define a control gate of the field-effect transistor;

forming conductive straps on sidewalls of the control gate and coupled to at least the first conductive layer and the second conductive layer;

removing portions of the first conductive layer and the gate dielectric layer adjacent the sidewalls of the control gate; and

forming source and drain regions in the substrate adjacent the sidewalls of the control gate.

48. A method of forming a floating-gate field-effect transistor, comprising:

forming a tunnel dielectric layer overlying a substrate;

forming a first conductive layer overlying the tunnel dielectric layer;

forming an interlayer dielectric layer overlying the first conductive layer;

forming a second conductive layer overlying the interlayer dielectric layer;

forming a cap layer overlying the second conductive layer;

patterning the cap layer and the second conductive layer to define a control gate of the floating-gate field-effect transistor;

forming conductive straps on sidewalls of the control gate and coupled to the second conductive layer;

removing portions of the interlayer dielectric layer, the first conductive layer and the tunnel dielectric layer adjacent the sidewalls of the control gate; and

forming source and drain regions in the substrate adjacent the sidewalls of the control gate.

49. A method of concurrently forming a field-effect transistor and a floating-gate field-effect transistor in an integrated circuit device, the method comprising:

forming a first dielectric layer overlying a substrate of the integrated circuit device;

forming a first conductive layer overlying the first dielectric layer;

forming a second dielectric layer overlying the first conductive layer;

forming a second conductive layer overlying the second dielectric layer;

removing portions of the second conductive layer to define control gates for the field-effect transistor and the floating-gate field-effect transistor;

removing portions of the second dielectric layer adjacent the control gate of the field-effect transistor while leaving portions of the second dielectric layer adjacent the control gate of the floating-gate field-effect transistor in place;

forming conductive straps overlying sidewalls of the control gates of the field-effect transistor and the floating-gate field-effect transistor, wherein the conductive straps extend from the first conductive layer to at least the second conductive layer in the control gate of the field-effect transistor and from the second dielectric layer to at least the second conductive layer in the control gate of the floating-gate field-effect transistor;

removing the portions of the second dielectric layer adjacent the control gate of the floating-gate field-effect transistor; and

removing portions of the first conductive layer adjacent the field-effect transistor and the floating-gate field-effect transistor.

50. The method of claim 49, further comprising forming a cap layer on the second conductive layer.

51. The method of claim 50, wherein the conductive straps extend to the cap layer.

52. The method of claim 49, wherein the first conductive layer is a polysilicon layer.

53. The method of claim 52, wherein the polysilicon layer is a conductively doped polysilicon layer.

54. The method of claim 49, wherein the second conductive layer comprises more than one conductive material.

55. The method of claim 49, wherein the second conductive layer comprises a metal-containing layer overlying a polysilicon layer.

56. The method of claim 55, wherein the metal-containing layer is a metal silicide layer.

57. The method of claim 49, wherein forming the conductive straps comprises blanket depositing conductive material and anisotropically removing portions of the conductive material to leave the straps on the sidewalls.

58. A method of concurrently forming a field-effect transistor and a floating-gate field-effect transistor in an integrated circuit device, the method, comprising:

forming a first dielectric layer overlying a substrate of the integrated circuit device;

forming a first polysilicon layer overlying the first dielectric layer;

forming a second dielectric layer overlying the first polysilicon layer;

forming a second polysilicon layer overlying the second dielectric layer;

forming a metal-containing layer overlying the second polysilicon layer;

forming a cap layer overlying the metal-containing layer;

removing portions of the second polysilicon layer, the metal-containing layer, and the cap layer to define control gates for the field-effect transistor and the floating-gate field-effect transistor;

removing portions of the second dielectric layer adjacent the control gate of the field-effect transistor while leaving portions of the second dielectric layer adjacent the control gate of the floating-gate field-effect transistor in place;

blanket depositing conductive material and anisotropically removing portions of the conductive material to leave conductive straps overlying sidewalls of the control gates of the field-effect transistor and the floating-gate field-effect transistor, wherein the conductive straps extend from the first polysilicon layer to at least the second polysilicon layer in the control gate of the field-effect transistor and from the second dielectric layer to at least the second polysilicon layer in the control gate of the floating-gate field-effect transistor;

removing the portions of the second dielectric layer adjacent the control gate of the floating-gate field-effect transistor; and

removing portions of the first polysilicon layer adjacent the field-effect transistor and the floating-gate field-effect transistor.

59. A method of forming a portion of a NAND memory array, comprising:

forming a plurality of columns of NAND strings of memory cells connected to select gates, the select gates of the respective columns interconnected by a

select line, wherein forming each of the select gates and the select line comprises:

separating first and second conductive layers of each of the select gates and the select line with an interlayer dielectric layer; and

electrically connecting the first and second conductive layers using opposing conductive straps formed on either side of the first and second conductive layers and interlayer dielectric layer, the pair of opposing straps spanning two or more of the plurality of columns.

60. The method of claim 59, further comprising forming the first conductive layer on a gate dielectric layer overlying a substrate.

61. The method of claim 60, further comprising forming a metal-containing layer overlying the second conductive layer before forming the opposing straps.

62. The method of claim 61, further comprising forming a cap layer on the metal-containing layer before forming the opposing straps.

63. A method of forming a portion of a NAND memory array, comprising:

forming a plurality of columns of NAND strings of memory cells connected between source select gates and drain select gates, wherein forming each of the source and drain select gates and each of the memory cells comprises:

forming a first dielectric layer on a substrate;

forming a first polysilicon layer on the first dielectric layer;

forming asecond dielectric layer on the first polysilicon layer;

forming a second polysilicon layer on the second dielectric layer;

forming a metal-containing layer on the second polysilicon layer; and

forming a cap layer on the metal-containing layer;

wherein forming each of the source and drain select gates further comprises forming a pair of opposing first conductive straps on each of opposing sidewalls of each of the source and drain select gates, wherein each first conductive strap electrically interconnects the first and second polysilicon layers, the pair of opposing first conductive straps spanning two or more of the plurality of columns; and

wherein forming each of the memory cells further comprises forming a pair of opposing second conductive straps on each of opposing sidewalls of each of the memory cells, wherein each second conductive strap contacts the metal-containing layer and the second polysilicon layer and extends from substantially an upper surface of the cap layer to the second dielectric layer, the pair of opposing second conductive straps spanning two or more of the plurality of columns.

64. A method of forming a portion of a memory device, comprising:

forming a first structure corresponding to a field-effect transistor and a plurality of second structures, each second structure corresponding to a floating-gate memory cell, wherein the first structure and the second structures overlay afirst dielectric layer formed on a first conductive layer, the first conductive layer formed on a second dielectric layer that is formed on a substrate, the first structure and each of the second structures comprising:

a second conductive layer formed on the first dielectric layer;

a third conductive layer formed on the second conductive layer; and

a cap layer formed on the third conductive layer;

masking the second structures and portions of the interlayer dielectric layer adjacent the second structures so as to leave portions of the first dielectric layer adjacent the first structure exposed;

removing the exposed portions of the first dielectric layer, thereby exposing portions of the first conductive layer adjacent the first structure;

forming a fourth conductive layer overlying the exposed portions of the first conductive layer adjacent the first structure, the first structure, the second structures, and the portions of the first dielectric layer adjacent the second structures;

selectively removing the fourth conductive layer so a portion of the fourth conductive layer remains on opposing sidewalls of the first structure and on opposing sidewalls of each of the second structures, wherein the portion of the fourth conductive layer remaining on the opposing sidewalls of the first structure forms opposing first conductive straps that extend substantially from an upper surface of the cap layer of the first structure to the first conductive layer adjacent the first structure, thereby electrically interconnecting the first conductive layer and the second conductive layer of the first structure, and wherein the portion of the fourth conductive layer remaining on the opposing sidewalls of each of the second structures forms opposing second conductive straps that extend substantially from an upper surface of the cap layer of each of the second structures to the first dielectric layer adjacent each of the second structures;

removing any portions of the first dielectric layer not underlying the cap layer of each of the second structures and not underlying the second conductive straps of each of the second structures; and

removing any portions of the first conductive layer not underlying the cap layer of the first structure and each of the second structures and not underlying the first conductive straps of the first structure and the second conductive straps of each of the second structures.

65. The method of claim 64, wherein the first and second conductive layers are polysilicon layers.

66. The method of claim 64, wherein the third conductive layer comprises a refractory metal silicide.

67. The method of claim 64, wherein the fourth conductive layer of a refractory metal silicide.

69. The method of claim 64, wherein cap layer is a layer of tetraethylorthosilicate.

70. The method of claim 64, wherein selectively removing the fourth conductive layer further comprises an anisotropic etch.